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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/197,993	11/23/1998	STEVEN EUGENE LOVETTE		1952

23990 7590 05/19/2004

DOCKET CLERK
P.O. DRAWER 800889
DALLAS, TX 75380

EXAMINER

NGUYEN, DUSTIN

ART UNIT	PAPER NUMBER
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2154

DATE MAILED: 05/19/2004

17

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No. 09/197,993	Applicant(s) LOVETTE, STEVEN EUGENE	
	Examiner Dustin Nguyen	Art Unit 2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 26-49 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 26-49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 26 – 49 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 26-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. [US Patent No 6,006,323], in view of Selesky et al. [US Patent No 5,890,181].

4. As per claim 26, Ma discloses the invention substantially as claimed including a method for detecting corruption associated with a stack in storage device, the method comprising the steps of:

detecting the occurrence of a stack operation within the stack [Abstract; and col 4, lines 10-15]; and

comparing the value in the first address location to the first predetermined value to determine if the stack operation corrupted the first predetermined value stored in the first address location [col 13, lines 13-22].

Ma does not specifically disclose

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storing a first predetermined value in a first address location immediately preceding the starting location of the stack.

Selesky discloses

storing a first predetermined value in a first address location immediately preceding the starting location of the stack [34a, 36a, Figure 4; and col 6, lines 59-65].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Ma and Selesky because Selesky's teaching would allow to manage stack in a more efficient manner.

5. As per claim 27, Ma discloses the first determined value comprises a known bit pattern [i.e. TOS] [col 9, lines 10-15].

6. As per claim 28, Ma discloses wherein the first predetermined value comprises a processor readable address [col 10, lines 20-28].

7. As per claim 29, Ma discloses wherein the first predetermined value comprises a processor readable instruction [col 6, lines 63-col 7, lines 6].

8. As per claims 30 and 31, Ma does not specifically discloses wherein the stack operation inserts data in the stack and removes data from the stack. Selesky discloses wherein the stack operation inserts data in the stack and removes data from the stack [Figure 4; and col 6, lines 59-col 7, lines 9]. It would have been obvious to a person skill in the art at the time the invention

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was made to combine the teaching of Ma and Selesky because Selesky's teaching would allow to maintain and control the push and pop of the stack [Selesky, col 2, lines 25-30].

9. As per claim 32, Ma does not disclose the step of storing a second predetermined value in a second address location immediately following the ending location of the stack. Selesky discloses the step of storing a second predetermined value in a second address location immediately following the ending location of the stack [40a, 42a, Figure 4; and col 6, lines 37-51]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Ma and Selesky because Selesky's teaching would allow to detect any corruption in the stack to maintain consistency in the stack.

10. As per claim 33, Ma discloses the second predetermined value comprises a known bit pattern [i.e. BOS] [col 9, lines 10-15].

11. As per claim 34, Ma discloses wherein the second predetermined value comprises a processor readable address [col 10, lines 65-col 11, lines 6].

12. As per claim 35, Ma discloses wherein the second predetermined value comprises a processor readable instruction [col 6, lines 64-col 7, lines 6].

13. As per claims 36 and 37, they are rejected for similar reasons as stated above in claims 30 and 31.

14. As per claims 38-49, they are apparatus claimed of claims 26-37, they are rejected for similar reasons as stated above in claims 26-37.

15. Applicant's arguments with respect to claims 26-49 have been considered but are moot in view of the new ground(s) of rejection.


16. A shortened statutory period for response to this action is set to expire **3 (three) months and 0 (zero) days** from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 U.S.C 133, M.P.E.P 710.02, 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (703) 305-5321. The examiner can normally be reached on Monday – Friday (8:00 – 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (703) 305-8498.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directly to the receptionist whose telephone number is (703) 305-3900.

Dustin Nguyen

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100